FIG. 1A

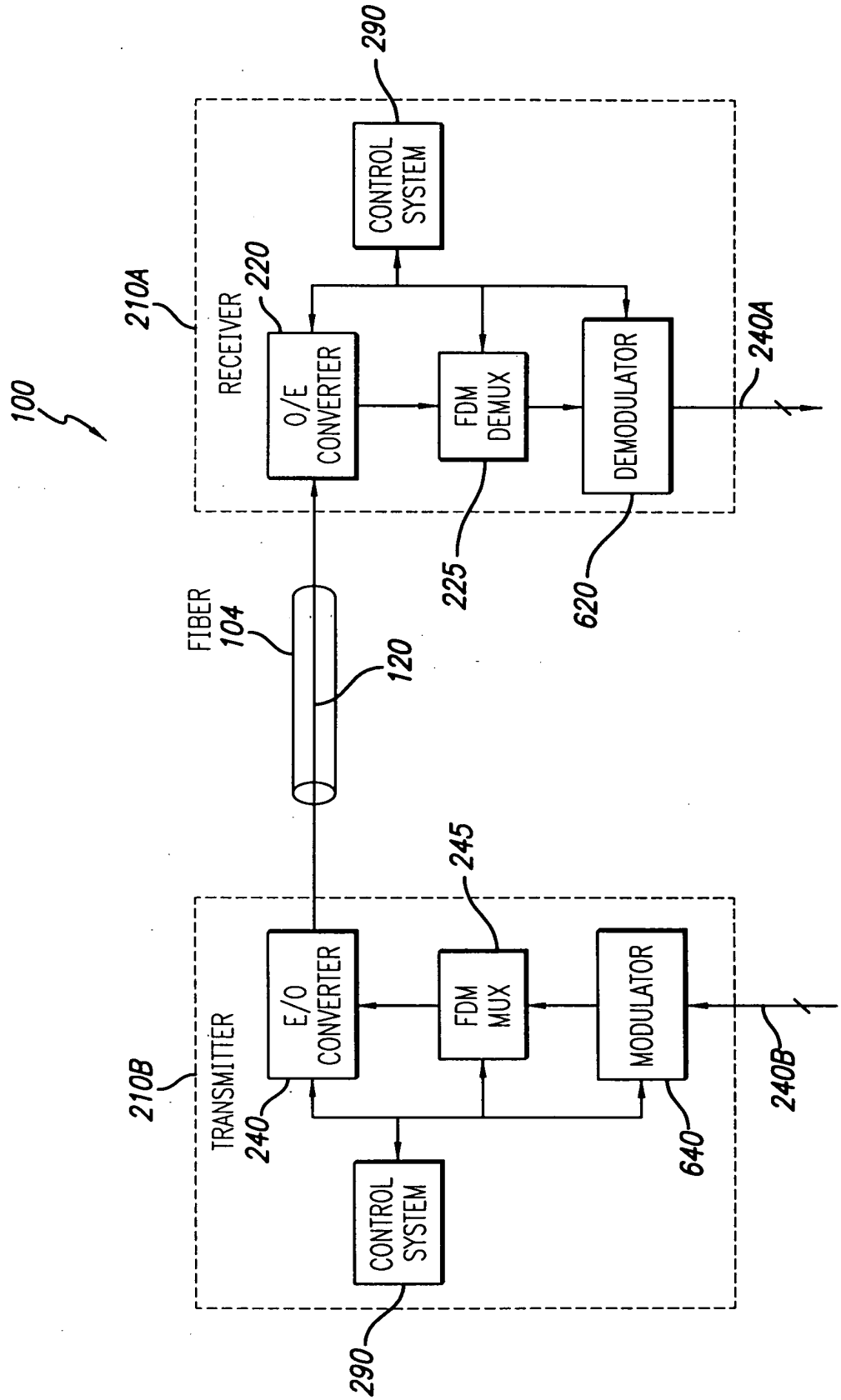

100
290
CONTROL SYSTEM
210A
RECEIVER
220
O/E CONVERTER
FDM DEMUX
DEMODULATOR
240A
225
620
FIBER
104
120
245
E/O CONVERTER
FDM MUX
MODULATOR
240B
210B
TRANSMITTER
240
640
CONTROL SYSTEM
290

FIG. 1B

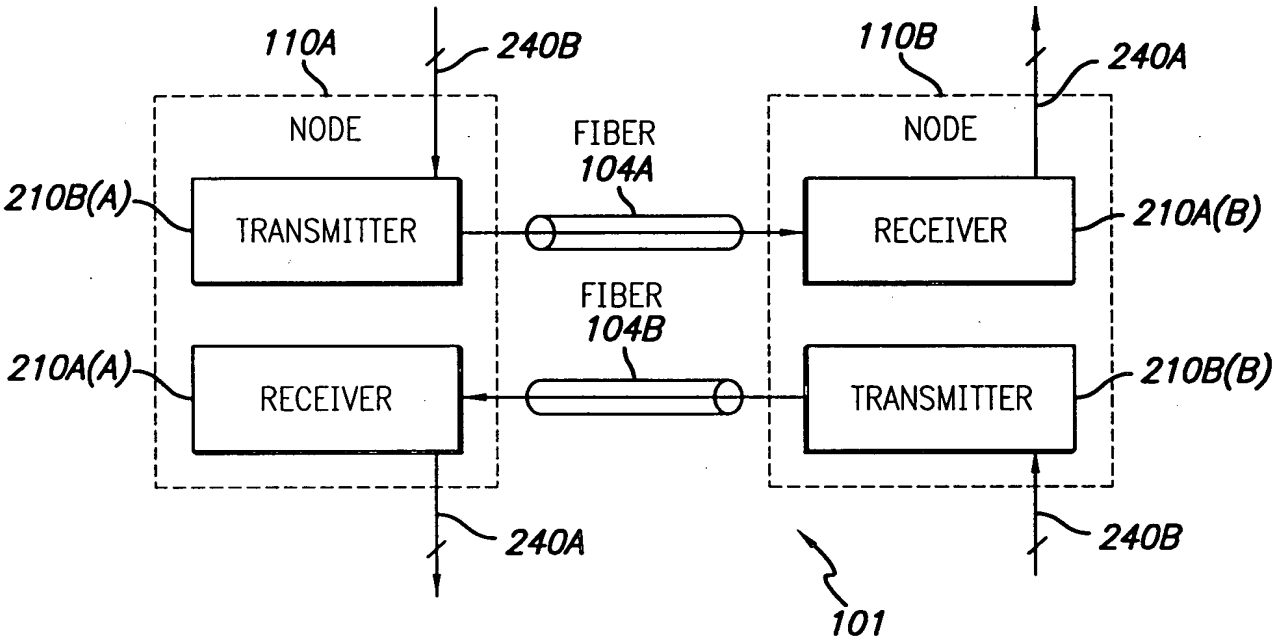

110A
240B
110B
240A
NODE
FIBER
104A
NODE
210B(A)
TRANSMITTER
RECEIVER
210A(B)
FIBER
104B
210A(A)
RECEIVER
TRANSMITTER
210B(B)
240A
240B
101

FIG. 2

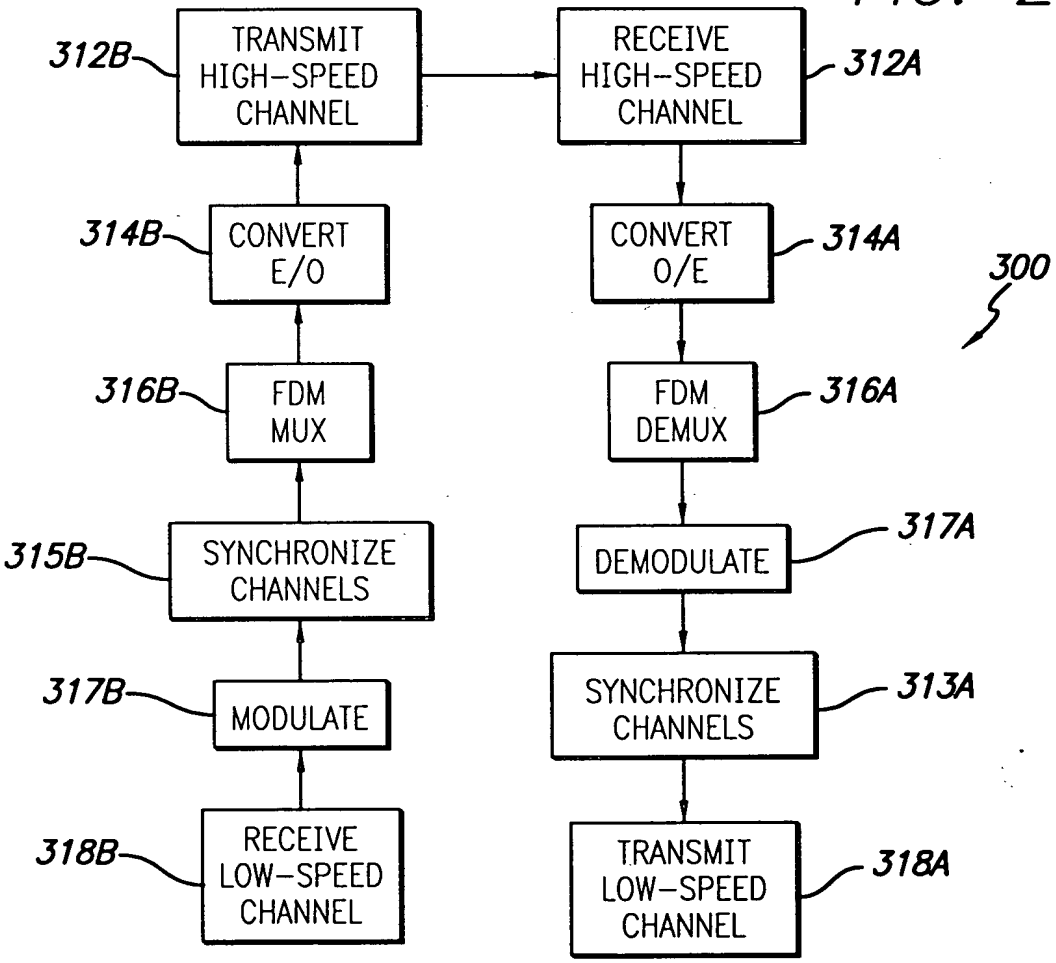

312B
TRANSMIT HIGH-SPEED CHANNEL
RECEIVE HIGH-SPEED CHANNEL
312A
314B
CONVERT E/O
CONVERT O/E
314A
300
316B
FDM MUX
FDM DEMUX
316A
315B
SYNCHRONIZE CHANNELS
DEMODULATE
317A
317B
MODULATE
SYNCHRONIZE CHANNELS
313A
318B
RECEIVE LOW-SPEED CHANNEL
TRANSMIT LOW-SPEED CHANNEL
318A

FIG. 3A

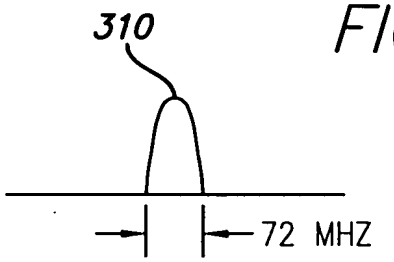


FIG. 3B

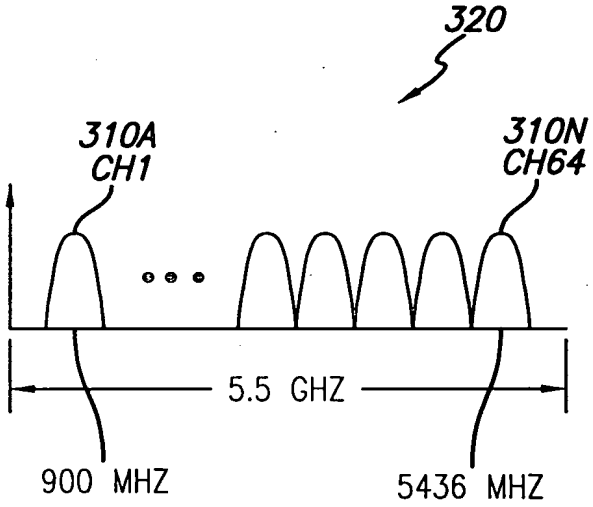
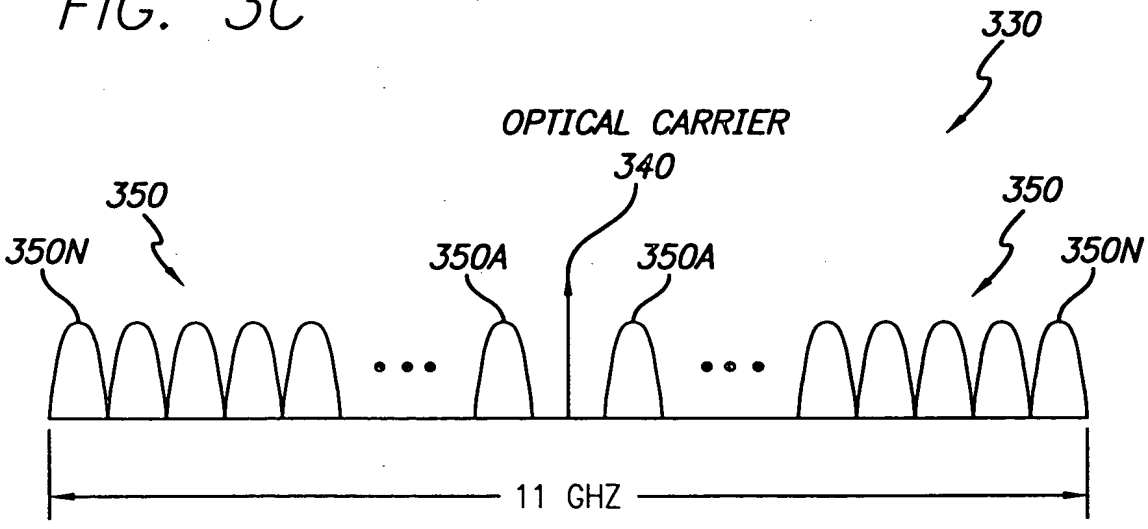


FIG. 3C



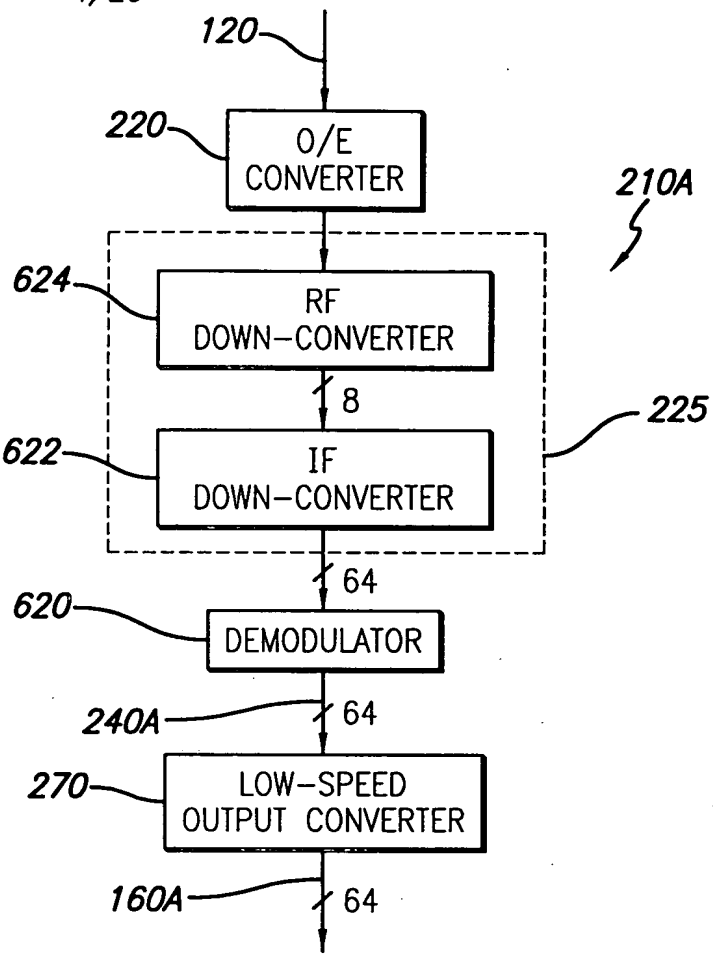

120
220
O/E CONVERTER
210A
624
RF DOWN-CONVERTER
8
225
622
IF DOWN-CONVERTER
64
620
DEMODULATOR
240A
64
270
LOW-SPEED OUTPUT CONVERTER
160A
64

FIG. 4A

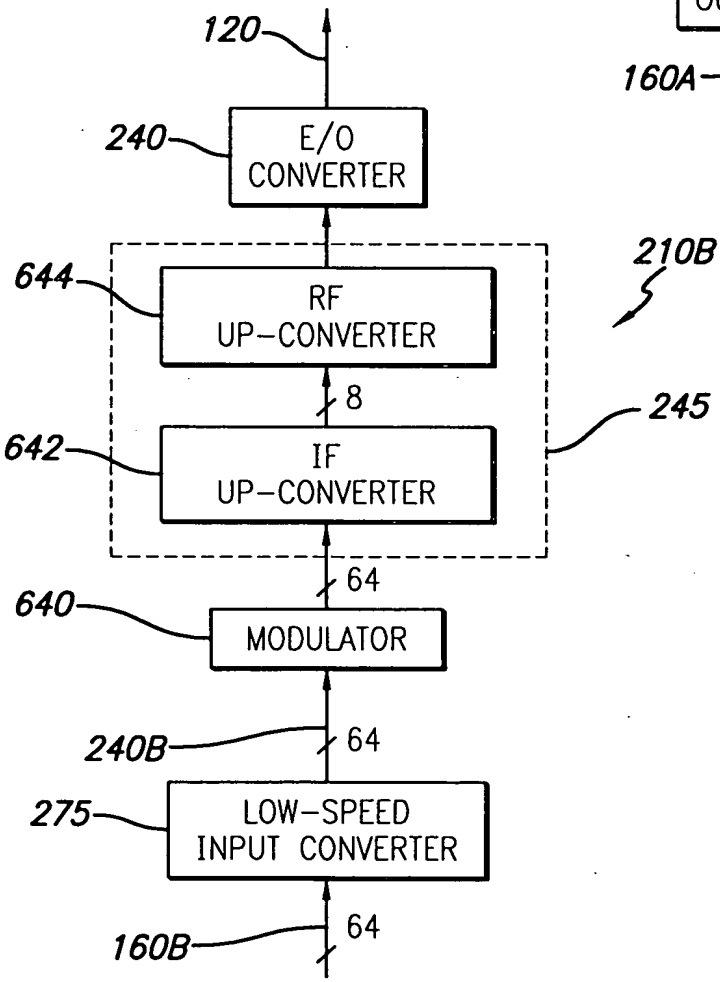

120
240
E/O CONVERTER
210B
644
RF UP-CONVERTER
8
245
642
IF UP-CONVERTER
64
640
MODULATOR
240B
64
275
LOW-SPEED INPUT CONVERTER
160B
64

FIG. 4B

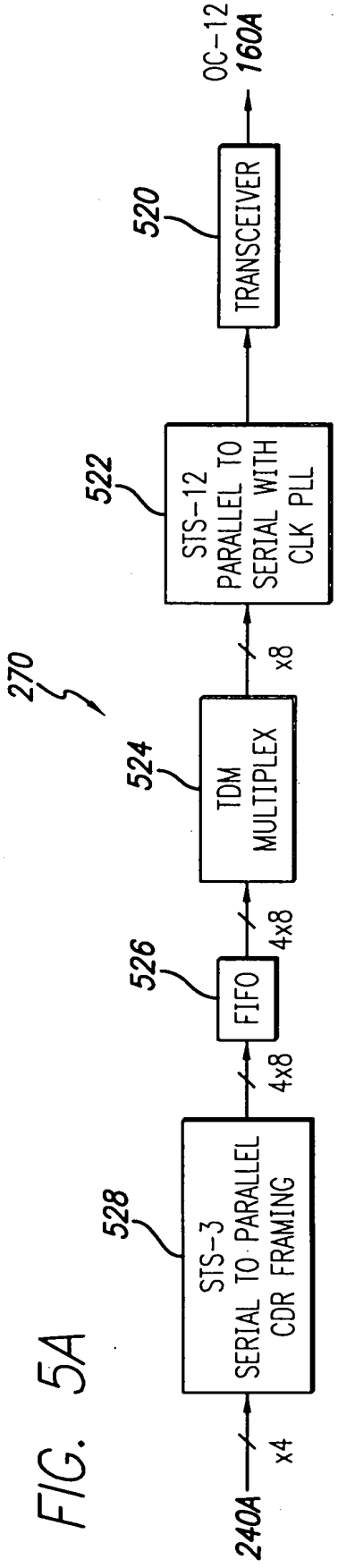

240A
x4
528
STS-3
SERIAL TO PARALLEL
CDR FRAMING
4x8
526
FIFO
4x8
524
TDM
MULTIPLEX
x8
270
522
STS-12
PARALLEL TO
SERIAL WITH
CLK PLL
520
TRANSCEIVER
OC-12
160A

FIG. 5A

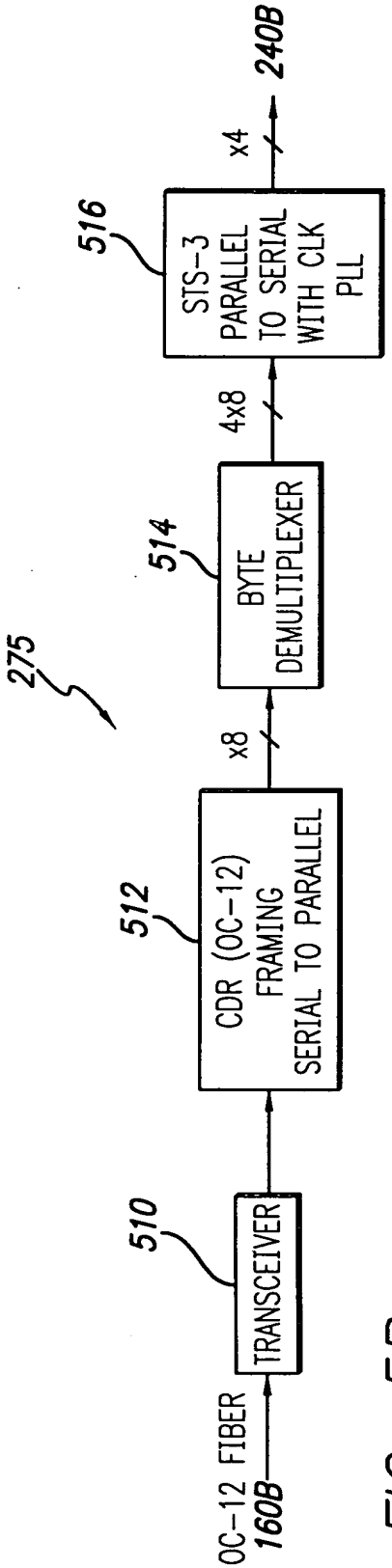

OC-12 FIBER
160B
510
TRANSCEIVER
512
CDR (OC-12)
FRAMING
SERIAL TO PARALLEL
x8
514
BYTE
DEMULTIPLEXER
4x8
275
516
STS-3
PARALLEL
TO SERIAL
WITH CLK
PLL
x4
240B

FIG. 5B

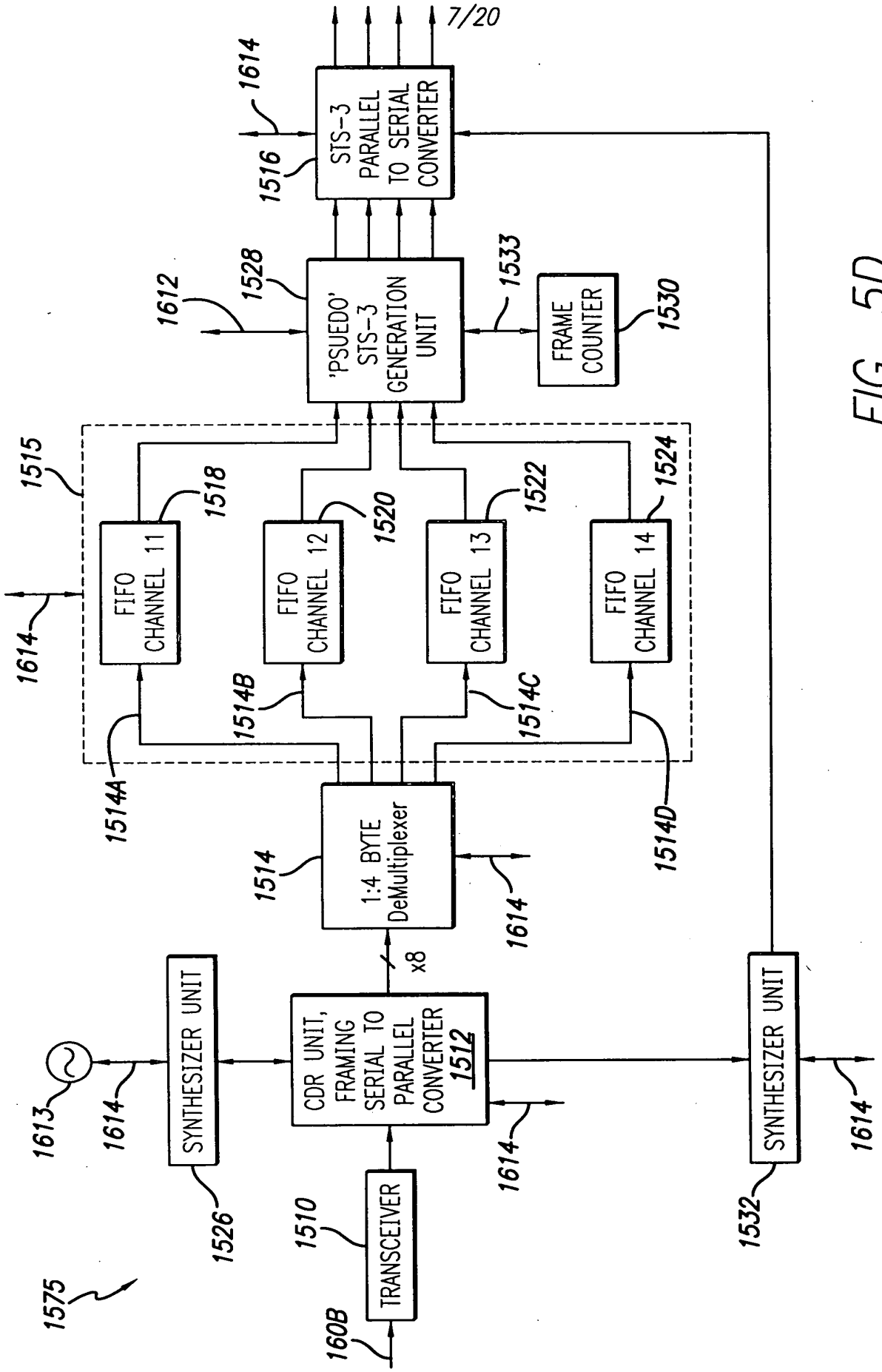

1614
STS-3 PARALLEL TO SERIAL CONVERTER
1516
1612
1528
'PSUEDO' STS-3 GENERATION UNIT
1533
FRAME COUNTER
1530
1515
1518
1520
1522
1524
FIFO CHANNEL 11
FIFO CHANNEL 12
FIFO CHANNEL 13
FIFO CHANNEL 14
1614
1514B
1514C
1514A
1514D
1514
1:4 BYTE DeMultiplexer
1614
x8
1613
1614
SYNTHESIZER UNIT
CDR UNIT, FRAMING SERIAL TO PARALLEL CONVERTER 1512
1614
SYNTHESIZER UNIT
1614
1526
1510
TRANSCEIVER
1532
1575
160B

FIG. 5D

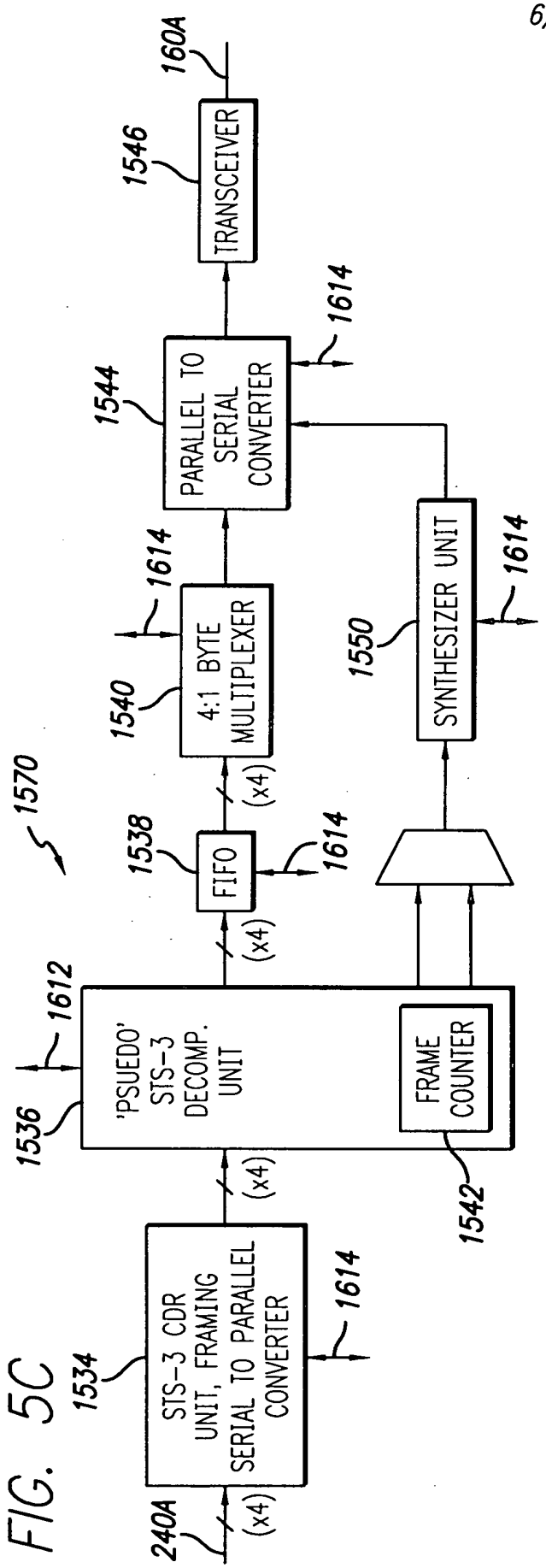

160A
1546
TRANSCEIVER
1544
PARALLEL TO SERIAL CONVERTER
1614
1540
4:1 BYTE MULTIPLEXER
(x4)
1538
FIFO
(x4)
1570
1536
'PSUEDO' STS-3 DECOMP. UNIT
1612
(x4)
1534
STS-3 CDR UNIT, FRAMING SERIAL TO PARALLEL CONVERTER
(x4)
240A
1550
SYNTHESIZER UNIT
FRAME COUNTER
1542

FIG. 5C

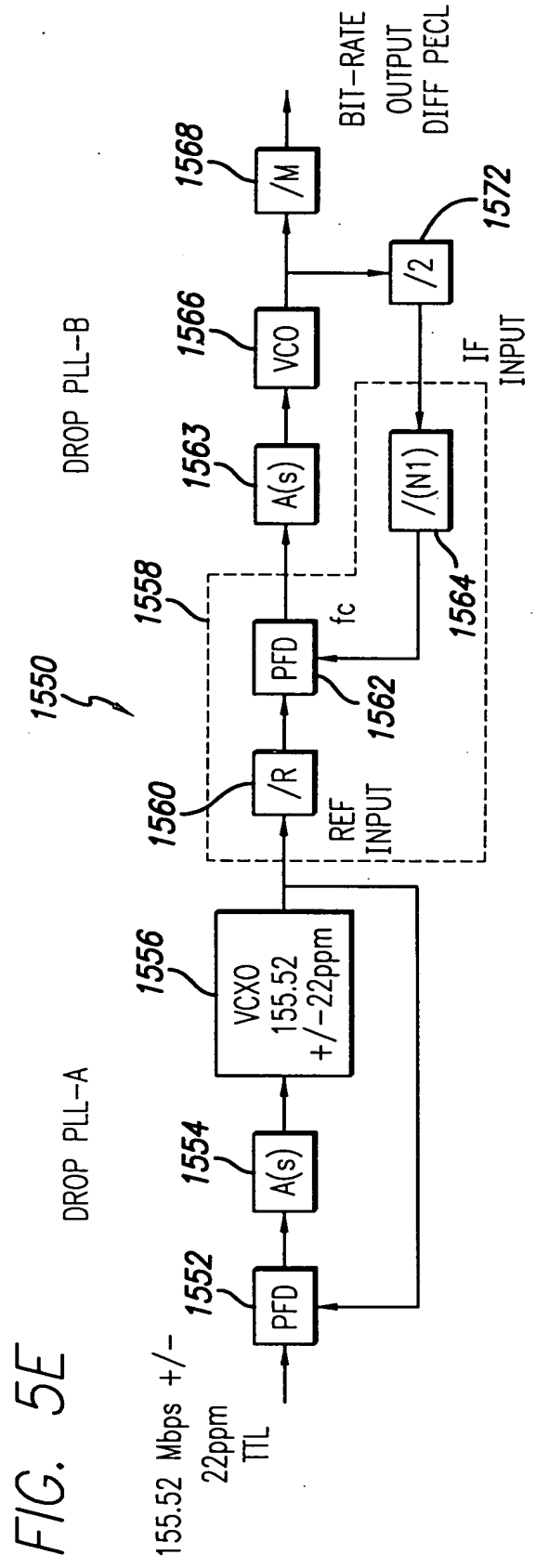

DROP PLL-A
DROP PLL-B
155.52 Mbps +/- 22ppm TTL
1552
PFD
1554
A(s)
1556
VCXO 155.52 +/-22ppm
1560
/R
REF INPUT
1558
PFD
fc
1562
1563
A(s)
1564
/(N1)
1566
VCO
1568
/M
BIT-RATE OUTPUT DIFF PECL
1572
/2
IF INPUT
1550

FIG. 5E

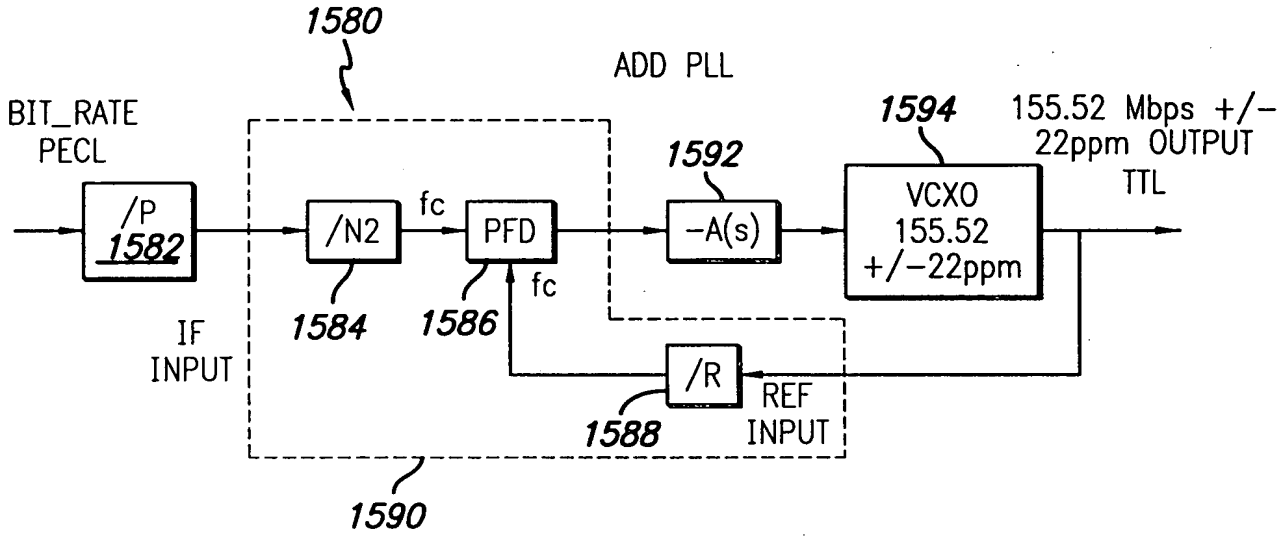

1580
ADD PLL
BIT_RATE
PECL
/P
1582
/N2
fc
PFD
fc
-A(s)
1592
1594
VCXO
155.52
+/-22ppm
155.52 Mbps +/-
22ppm OUTPUT
TTL
IF
INPUT
1584
1586
/R
REF
INPUT
1588
1590

FIG. 5F

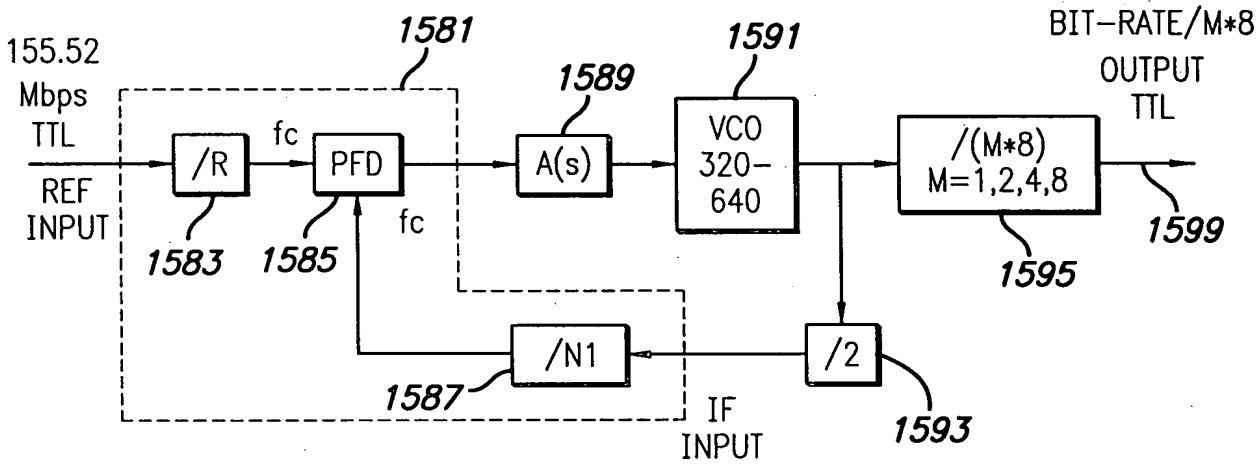

155.52
Mbps
TTL
REF
INPUT
1581
/R
fc
PFD
fc
1583
1585
1589
A(s)
1591
VCO
320-
640
/(M*8)
M=1,2,4,8
BIT-RATE/M*8
OUTPUT
TTL
1599
1595
/N1
1587
/2
1593
IF
INPUT

FIG. 5G

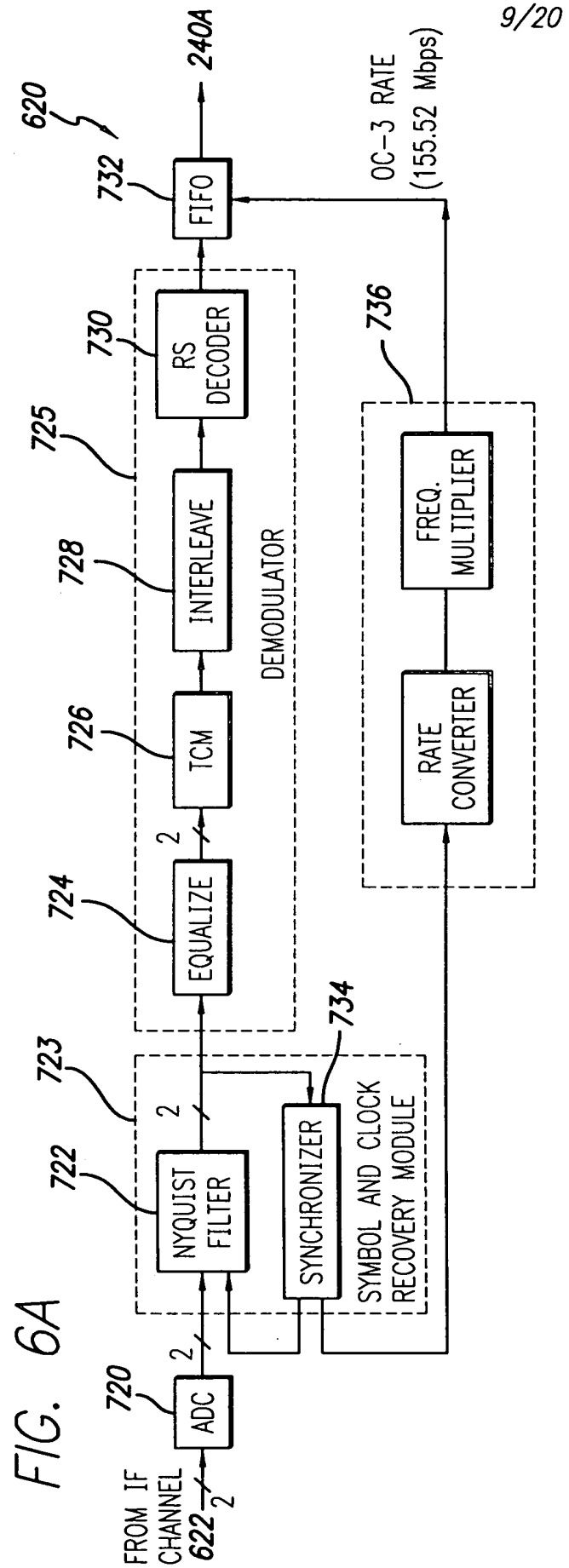

FROM IF CHANNEL
622
2
ADC
720
2
NYQUIST FILTER
722
2
723
SYNCHRONIZER
734
SYMBOL AND CLOCK RECOVERY MODULE
EQUALIZE
724
2
TCM
726
INTERLEAVE
728
RS DECODER
730
FIFO
732
240A
620
DEMODULATOR
725
RATE CONVERTER
FREQ. MULTIPLIER
736
OC-3 RATE (155.52 Mbps)

FIG. 6A

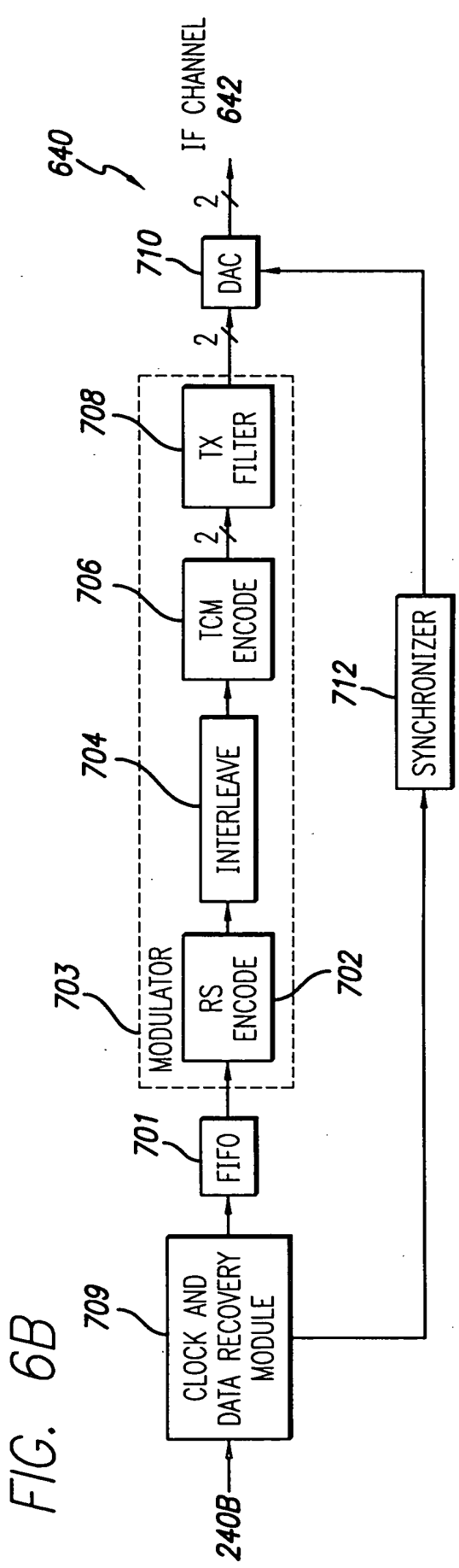

240B
CLOCK AND DATA RECOVERY MODULE
709
FIFO
701
2
RS ENCODE
702
703
MODULATOR
INTERLEAVE
704
TCM ENCODE
706
2
TX FILTER
708
2
DAC
710
2
IF CHANNEL
642
640
SYNCHRONIZER
712

FIG. 6B

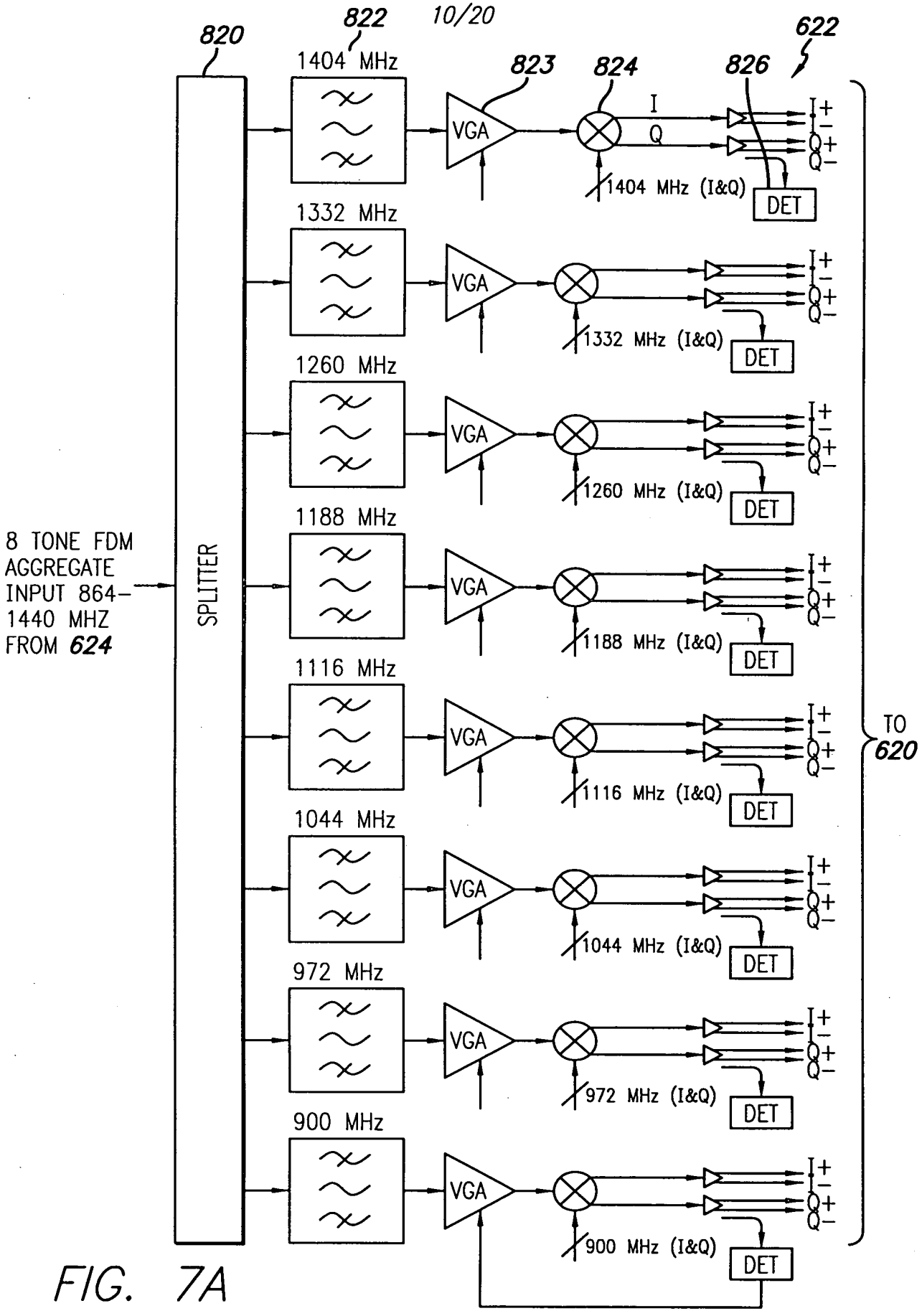

820
822
823
824
826
622
1404 MHz
1332 MHz
1260 MHz
1188 MHz
1116 MHz
1044 MHz
972 MHz
900 MHz
VGA
I
Q
1404 MHz (I&Q)
1332 MHz (I&Q)
1260 MHz (I&Q)
1188 MHz (I&Q)
1116 MHz (I&Q)
1044 MHz (I&Q)
972 MHz (I&Q)
900 MHz (I&Q)
DET
I+
I−
Q+
Q−
SPLITTER
8 TONE FDM AGGREGATE INPUT 864– 1440 MHZ FROM 624
TO 620

FIG. 7A

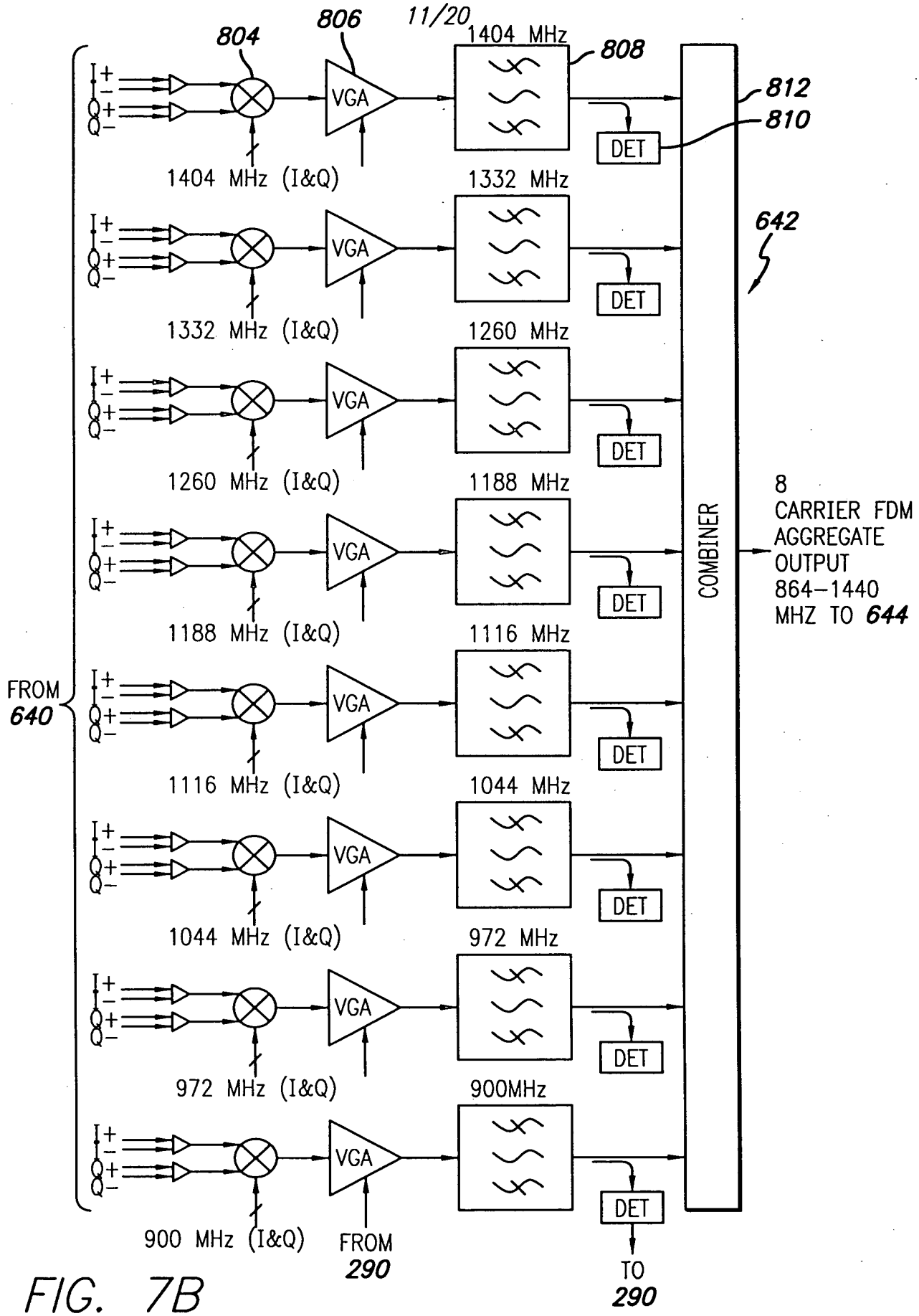

804
806
11/20
1404 MHz
808
812
810
VGA
DET
1404 MHz (I&Q)
1332 MHz
642
1332 MHz (I&Q)
1260 MHz
1260 MHz (I&Q)
1188 MHz
1188 MHz (I&Q)
1116 MHz
1116 MHz (I&Q)
1044 MHz
1044 MHz (I&Q)
972 MHz
972 MHz (I&Q)
900MHz
900 MHz (I&Q)
FROM 290
TO 290
FROM 640
COMBINER
8 CARRIER FDM AGGREGATE OUTPUT 864–1440 MHZ TO 644

FIG. 7B

FIG. 8A

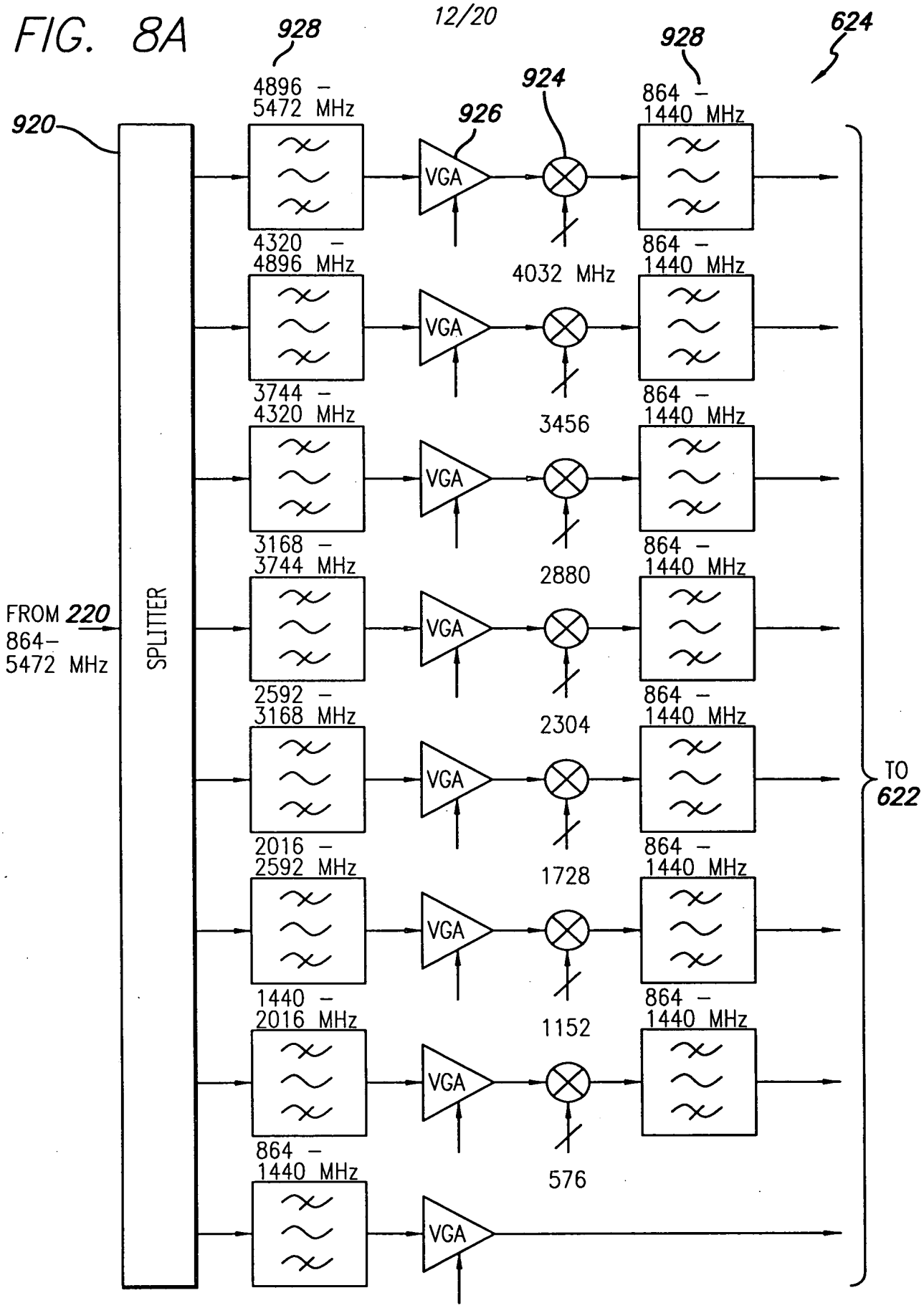
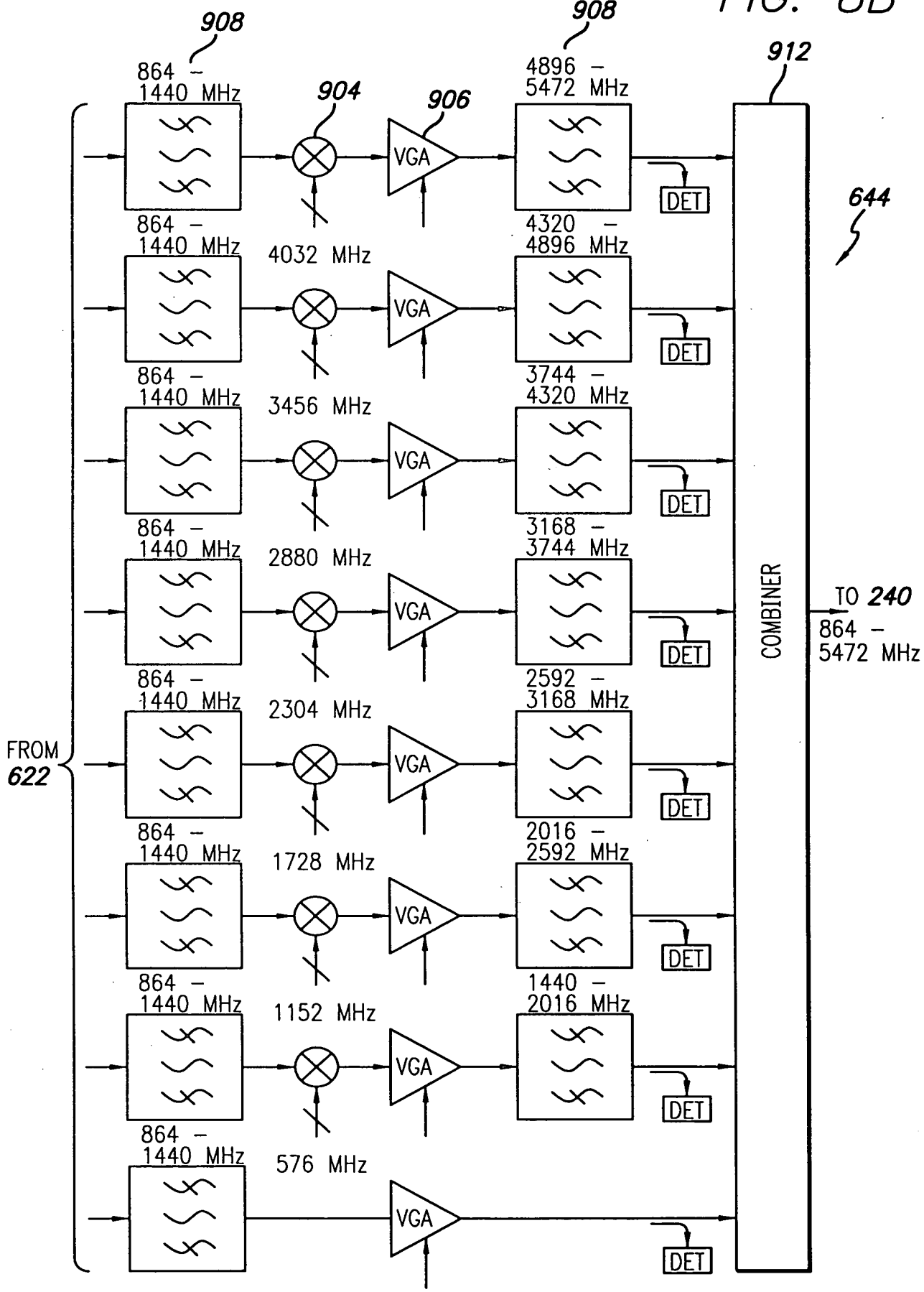
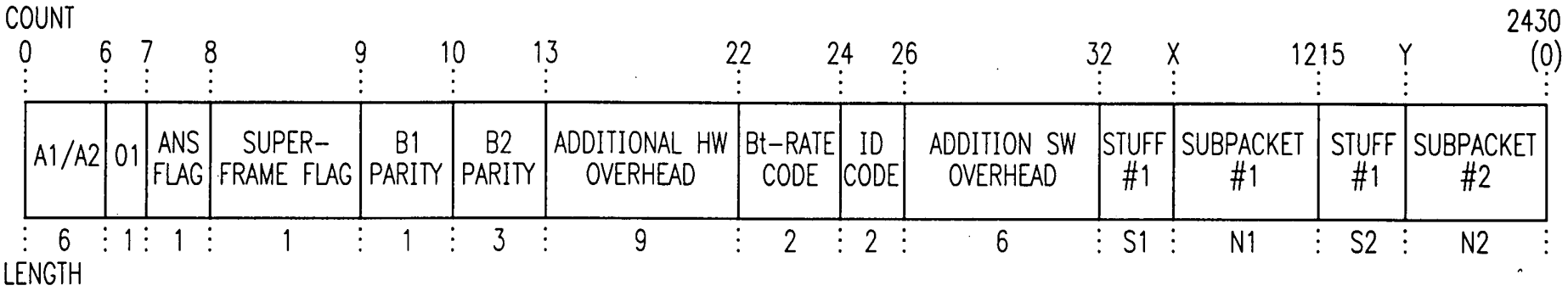

928
624
928
924
926
920
4896 – 5472 MHz
864 – 1440 MHz
VGA
4320 – 4896 MHz
4032 MHz
3744 – 4320 MHz
3456
3168 – 3744 MHz
2880
2592 – 3168 MHz
2304
2016 – 2592 MHz
1728
1440 – 2016 MHz
1152
864 – 1440 MHz
576
FROM 220
864– 5472 MHz
SPLITTER
TO 622

FIG. 8B


908
908
912
904
906
644
FROM 622
TO 240
864 – 1440 MHz
4896 – 5472 MHz
4032 MHz
4320 – 4896 MHz
3456 MHz
3744 – 4320 MHz
2880 MHz
3168 – 3744 MHz
2304 MHz
2592 – 3168 MHz
1728 MHz
2016 – 2592 MHz
1152 MHz
1440 – 2016 MHz
576 MHz
VGA
DET
COMBINER
864 – 5472 MHz



A1/A2 bytes-SONETheader for STS3.

Additional SW Overhead-6bytes

Additional HW Overhead-9bytes

Subpacket-target bytes carried in frame. Two subpackets to reduce system latency.

Stuff-stuff bytes to fill unused parts of packet.

Parity-1 byte parity for performance monitoring

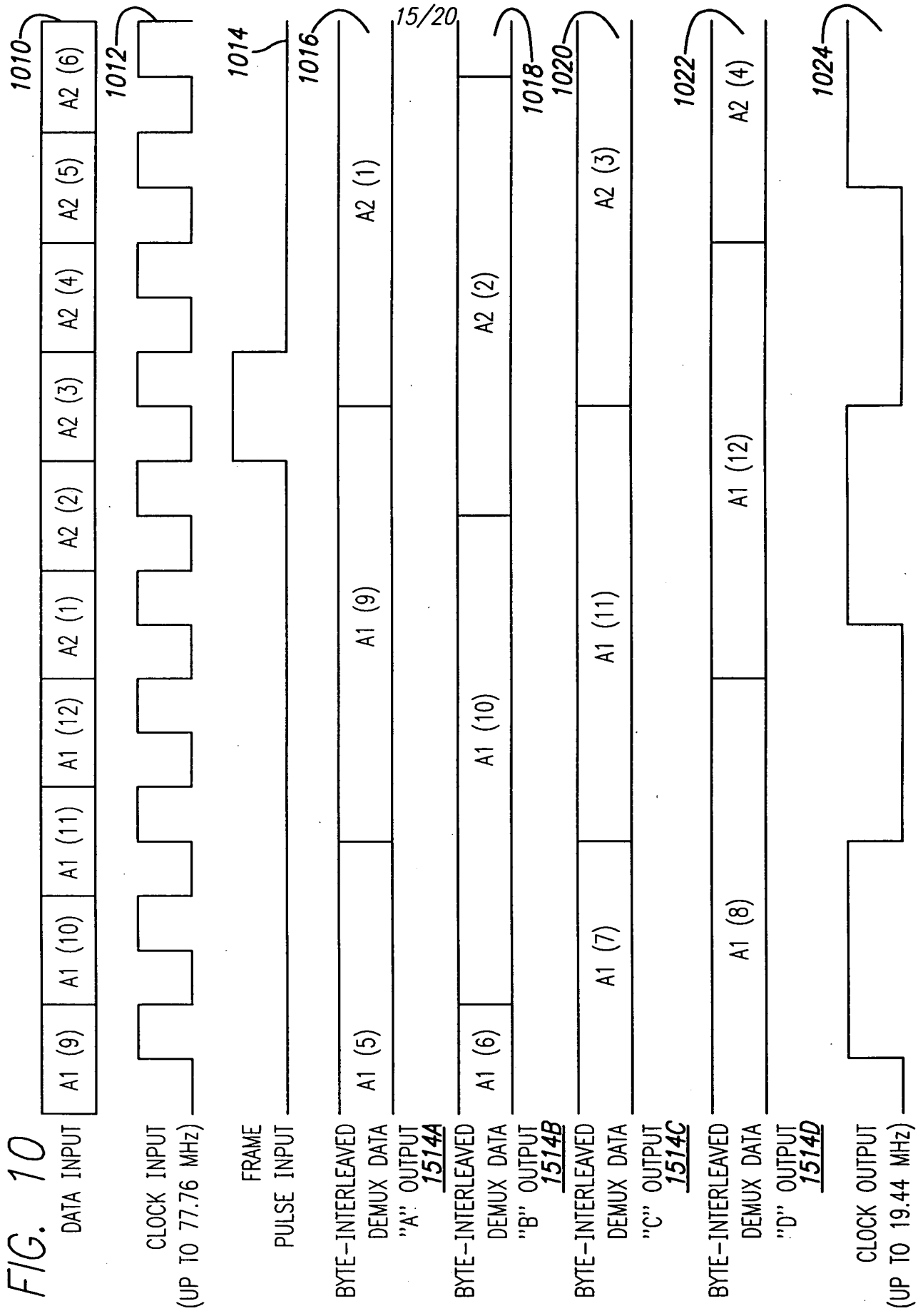
N1-subpacket 1 byte count
N2-subpacket 2 byte count
N1+N2=N(target signal bytes per frame)
S1-Stuff #1 byte count
S2-Stuff #2 byte count
X-Stuff #1 end count Memory mapped register
Y-Stuff #2 end count Memory Mapped register
T-Target Signal Data Rate

N=T/(8kHz)*(1/8)*(1/4) bytes/frame

S1+S2=2430-N-32 bytes/frame

FIG. 9

FIG. 10


1010
1012
1014
1016
1018
1020
1022
1024
DATA INPUT
A1 (9)
A1 (10)
A1 (11)
A1 (12)
A2 (1)
A2 (2)
A2 (3)
A2 (4)
A2 (5)
A2 (6)
CLOCK INPUT
(UP TO 77.76 MHz)
FRAME
PULSE INPUT
BYTE-INTERLEAVED
DEMUX DATA
"A" OUTPUT
1514A
A1 (5)
A1 (9)
A2 (1)
BYTE-INTERLEAVED
DEMUX DATA
"B" OUTPUT
1514B
A1 (6)
A1 (10)
A2 (2)
BYTE-INTERLEAVED
DEMUX DATA
"C" OUTPUT
1514C
A1 (7)
A1 (11)
A2 (3)
BYTE-INTERLEAVED
DEMUX DATA
"D" OUTPUT
1514D
A1 (8)
A1 (12)
A2 (4)
CLOCK OUTPUT
(UP TO 19.44 MHz)

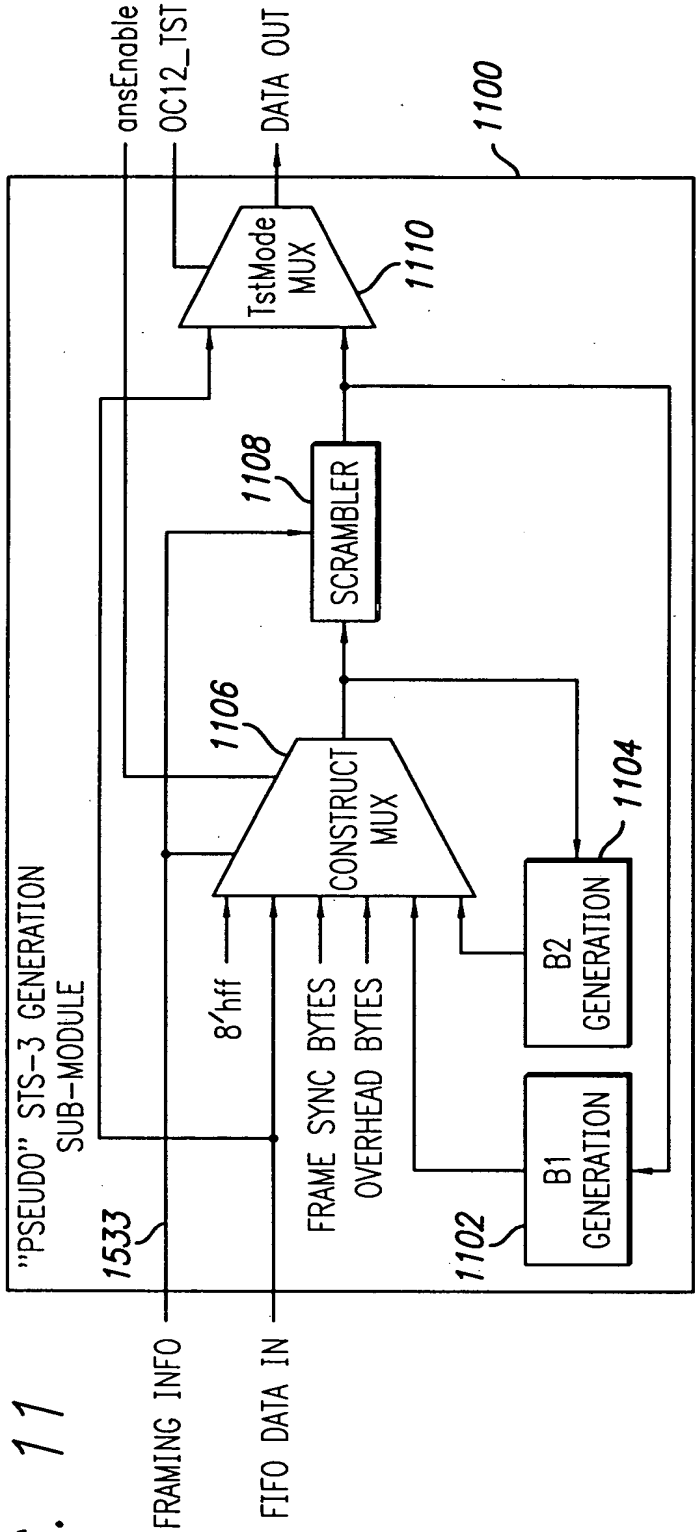

ansEnable
OC12_TST
DATA OUT
1100
TstMode MUX
1110
1108
SCRAMBLER
1106
CONSTRUCT MUX
1104
B2 GENERATION
B1 GENERATION
1102
"PSEUDO" STS-3 GENERATION SUB-MODULE
1533
8'hff
FRAME SYNC BYTES
OVERHEAD BYTES
FRAMING INFO
FIFO DATA IN

FIG. 11

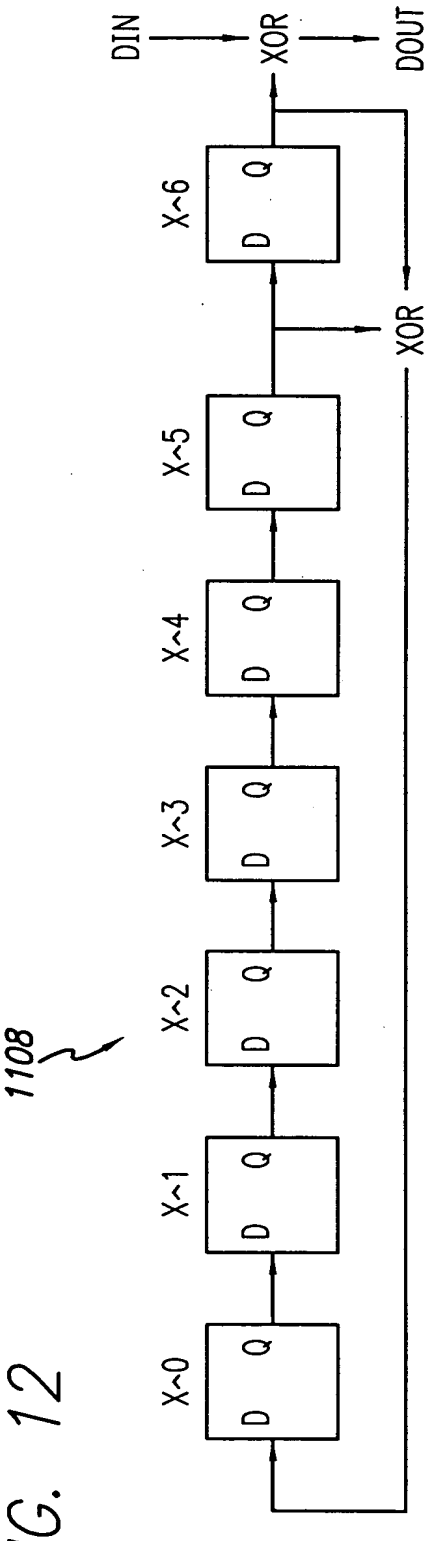

1108
DIN
XOR
DOUT
X^6
X^5
X^4
X^3
X^2
X^1
X^0
D Q
XOR

FIG. 12

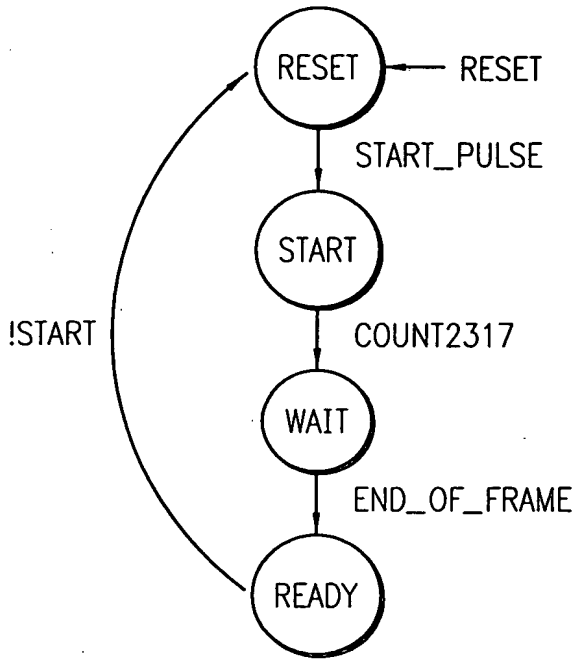

RESET
RESET
START_PULSE
START
!START
COUNT2317
WAIT
END_OF_FRAME
READY

FIG. 13

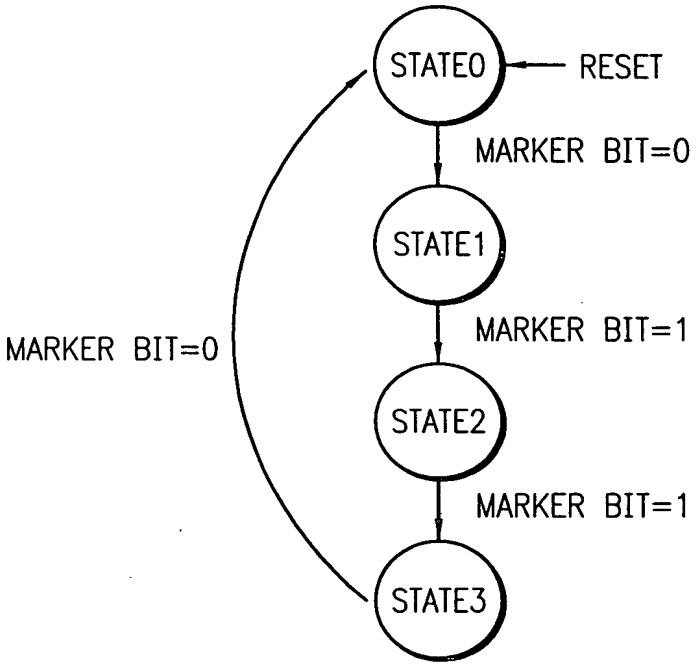

STATE0
RESET
MARKER BIT=0
STATE1
MARKER BIT=0
MARKER BIT=1
STATE2
MARKER BIT=1
STATE3

FIG. 14

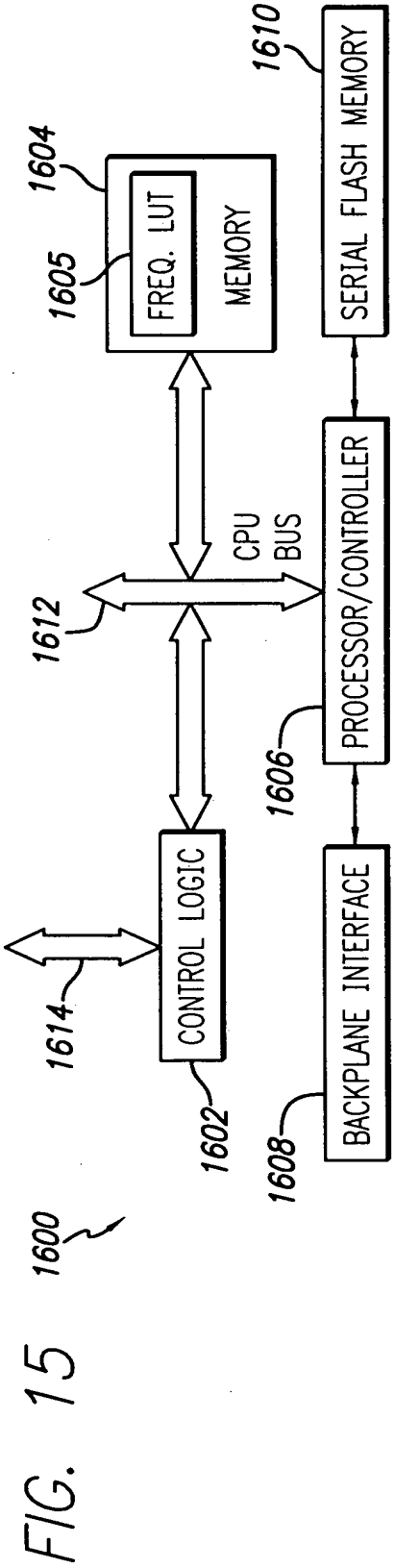

1600
1602
CONTROL LOGIC
1604
1605
FREQ. LUT
MEMORY
1606
PROCESSOR/CONTROLLER
1608
BACKPLANE INTERFACE
1610
SERIAL FLASH MEMORY
1612
CPU BUS
1614

FIG. 15

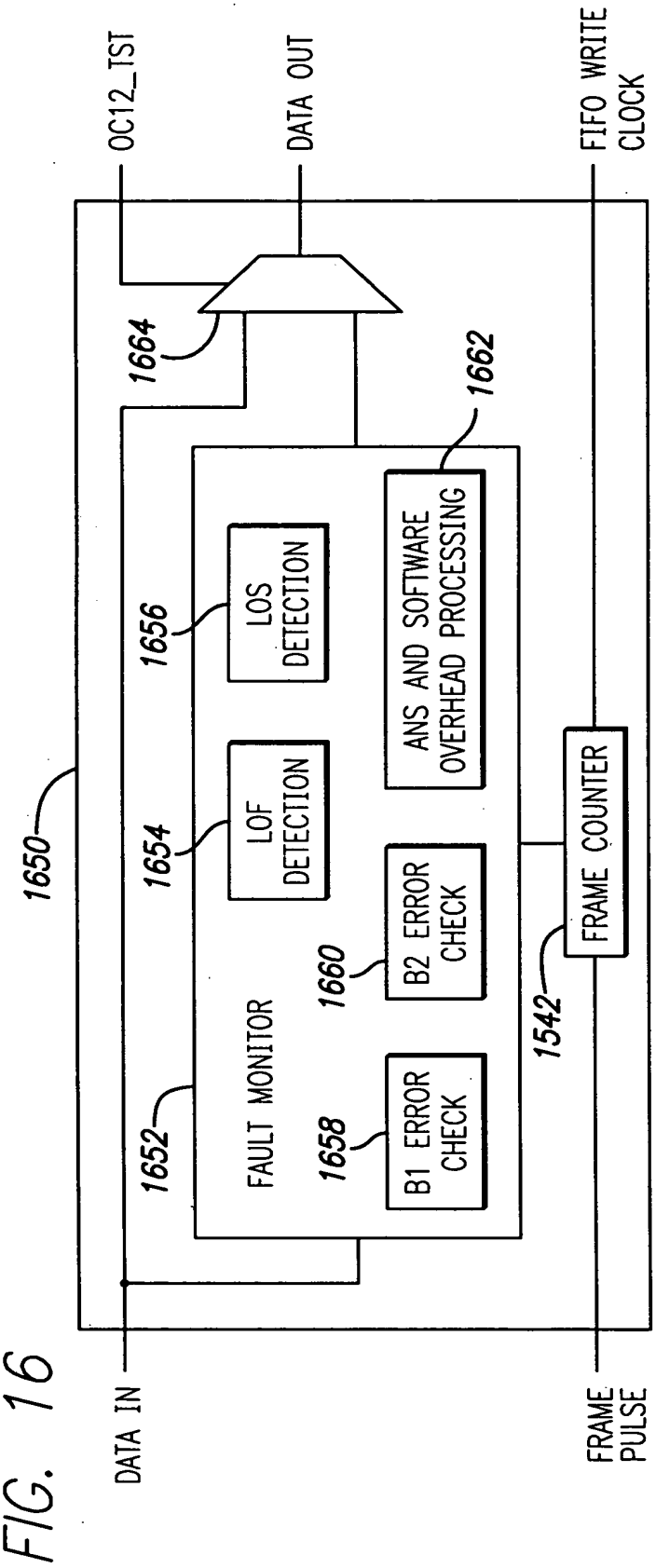

OC12_TST
DATA OUT
FIFO WRITE CLOCK
1650
1652
FAULT MONITOR
1654
LOF DETECTION
1656
LOS DETECTION
1658
B1 ERROR CHECK
1660
B2 ERROR CHECK
1662
ANS AND SOFTWARE OVERHEAD PROCESSING
1664
1542
FRAME COUNTER
DATA IN
FRAME PULSE

FIG. 16

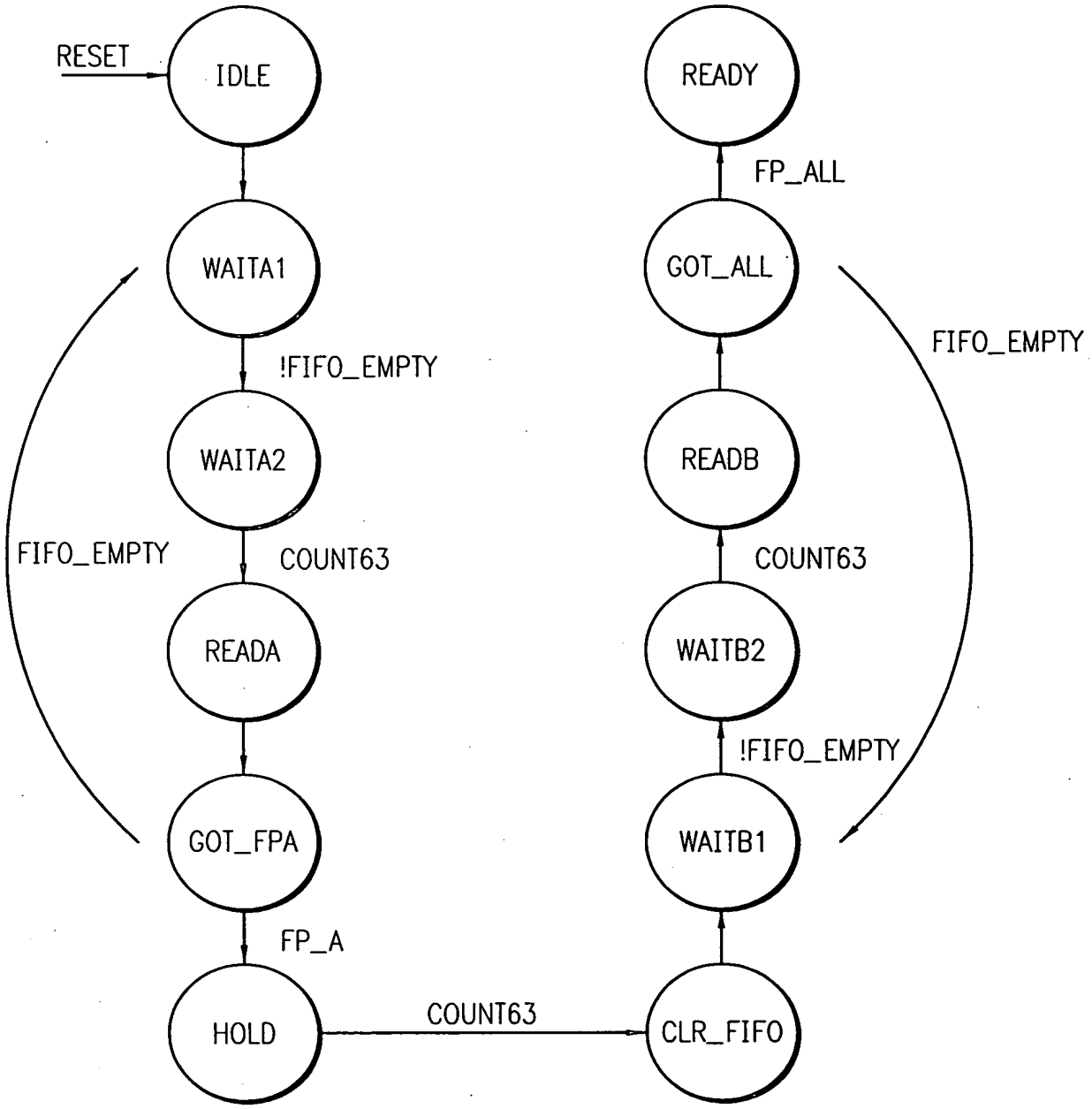
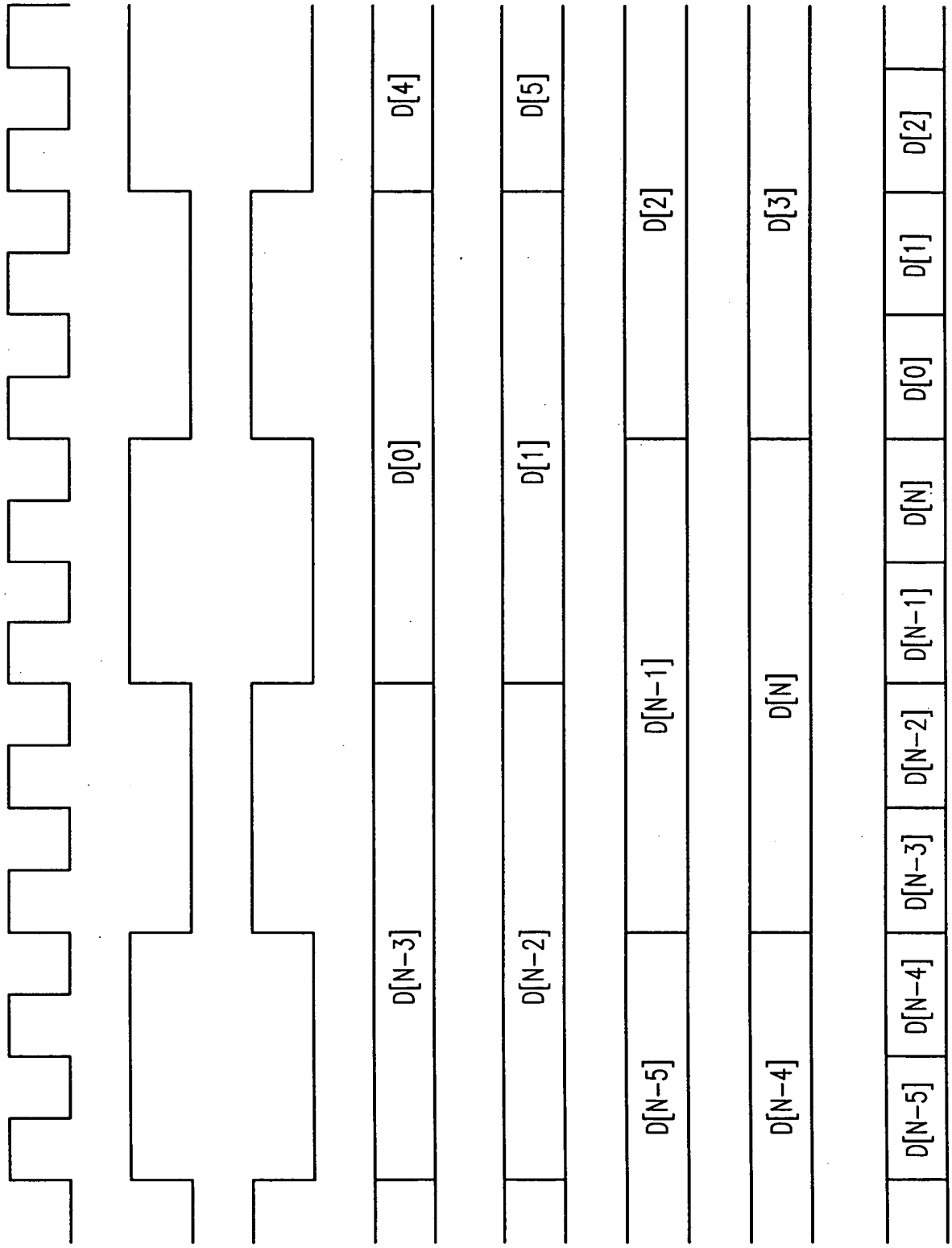

RESET
IDLE
WAITA1
!FIFO_EMPTY
WAITA2
FIFO_EMPTY
COUNT63
READA
GOT_FPA
FP_A
HOLD
COUNT63
CLR_FIFO
WAITB1
!FIFO_EMPTY
WAITB2
COUNT63
READB
GOT_ALL
FIFO_EMPTY
FP_ALL
READY

FIG. 17

FIG. 18


BYTE MUX CLOCK INPUT
FIFO A&B CLOCK INPUT
FIFO C&D CLOCK INPUT
FIFO "A" DATA OUTPUT
FIFO "B" DATA OUTPUT
FIFO "C" DATA OUTPUT
FIFO "D" DATA OUTPUT
BYTE MUX DATA OUTPUT
D[N-3]
D[0]
D[4]
D[N-2]
D[1]
D[5]
D[N-5]
D[N-1]
D[2]
D[N-4]
D[N]
D[3]
D[N-5]
D[N-4]
D[N-3]
D[N-2]
D[N-1]
D[N]
D[0]
D[1]
D[2]